CLAIMS

What is claimed is:

1. A method for providing a sinker on a semiconductor device comprising the steps of:

(a) providing a substrate region;

(b) providing a buried layer and an epitaxial (EPI) layer over the substrate region;

(c) etching a plurality of device structures in the EPI layer;

(d) providing a slot in the semiconductor substrate that is in contact with the buried layer and the substrate region;

(e) oxidizing the slot except at the bottom of the slot; and

(f) providing metal within the slot.

2. The method of claim 1 wherein the at least one metal providing step (f) comprises the step of:

(f1) filling the slot utilizing a metal that is provided on the surface of the EPI layer that is of a thickness that is one-half the depth or width of the at least one slot.

3. The method of claim 1 wherein the at least one metal comprises a plurality of metals.

4. The method of claim 3 wherein the plurality of metals comprises two meals, a

first metal covers one half the slot depth and a second metal fills the slot.

5. The method of claim 4 wherein the plurality of metals comprises three deposited metals, wherein the first and second metal depositions fill the slot followed by a deposited dielectric, wherein the dielectric has contacts opened above the slots and the third deposited metal provides an interconnect layer wherein the third metal forms the contacts to a circuit and the second deposited metal.

6. The method of claim 1 wherein the metal is provided utilizing chemical vapor deposition.

7. The method of claim 1 wherein the metal is provided utilizing sputter deposition.

8. The method of claim 1 wherein the sinker can be coupled to a collector or a drain of a device to ensure lowest resistance.

9. A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including a plurality of device structures thereon, and a buried layer in the semiconductor substrate; and

an interconnect on the semiconductor substrate, the interconnect comprising at least one slot provided in the semiconductor substrate and at least one metal within the slot, wherein the at least one slot is oxidized everywhere except at the bottom of the slot, and the

interconnect forms a sinker to the buried layer.

10. The semiconductor device of claim 9 wherein the metal comprises a plurality of metals.

11. The semiconductor device of claim 10 wherein the plurality of metals comprises two metals, a first metal covers one-half of the slot and a second metal fills the slot.

12. The semiconductor device of claim 11 wherein the plurality of metals comprises three metals, wherein the first and second metals fill the slot and the third metal provides an interconnect layer.

13. A high voltage interconnect on a semiconductor substrate, the substrate including a buried layer comprising:

a slot provided in the semiconductor substrate; and

at least one metal within the slot, wherein the at least one slot is oxidized everywhere except at the bottom of the slot, and the interconnect forms a sinker to the buried layer.

14. The interconnect of claim 13 wherein the metal comprises a plurality of metals.

15. The interconnect of claim 14 wherein the plurality of metals comprises two metals, a first metal covers one-half of the slot and a second metal fills the slot.

16. The interconnect of claim 14 wherein the plurality of metals comprises three metals, wherein the first and second meals fill the slot and the third metal provides an interconnect layer.

17. The interconnect of claim 12 wherein the sinker can be coupled to a collector on a drain of a device to ensure lowest resistance.

18. The interconnect of claim 16 wherein the slot with oxide completely around the three deposited layers is coupled to an emitter of a bipolar device which provides a high current carrying connection to the emitter.

19. The interconnect of claim 16 wherein the slot with oxide completely around the three deposited layers is coupled to a source MOS transistor which provides a high current carrying connection to the source.

20. The interconnect of claim 16 wherein there are a plurality of slots filled with three depositions of metal.

21. The interconnect of claim 20 wherein the plurality of slots are coupled to the emitters, collectors, drains, sources of Bipolar transistors and MOS transistors on the same device, thus forming high current carrying conductors on a same device while limiting the area consumed on the surface to a maximum width of a slot.

22. The interconnect of claim 21 wherein the high current carrying conductors are on the same level of metal resulting in thick metal obtained vertically in the substrate, while limiting the space on the surface of the device and not requiring additional planarization.